Lab Report-5

(Sanchit jalan,Group-3,2022101070,Table No:-40)

Experiment 5A:-

To assemble SR Latch using 2 NOR gates

Electronic components required:-

1. Digital test kit
2. Wires
3. NOR gates

Pin and logic gate diagram:-

Diagram, schematic

Description automatically generated

TinkerCAD screenshot:-

Timeline

Description automatically generated

Procedure:-

1. Connect the ICs with power supply and make appropriate connections in NOR gate using the above given pin diagram
2. Cross connect the outputs to make a perfect RS latch
3. Check the outputs and tabulate them.

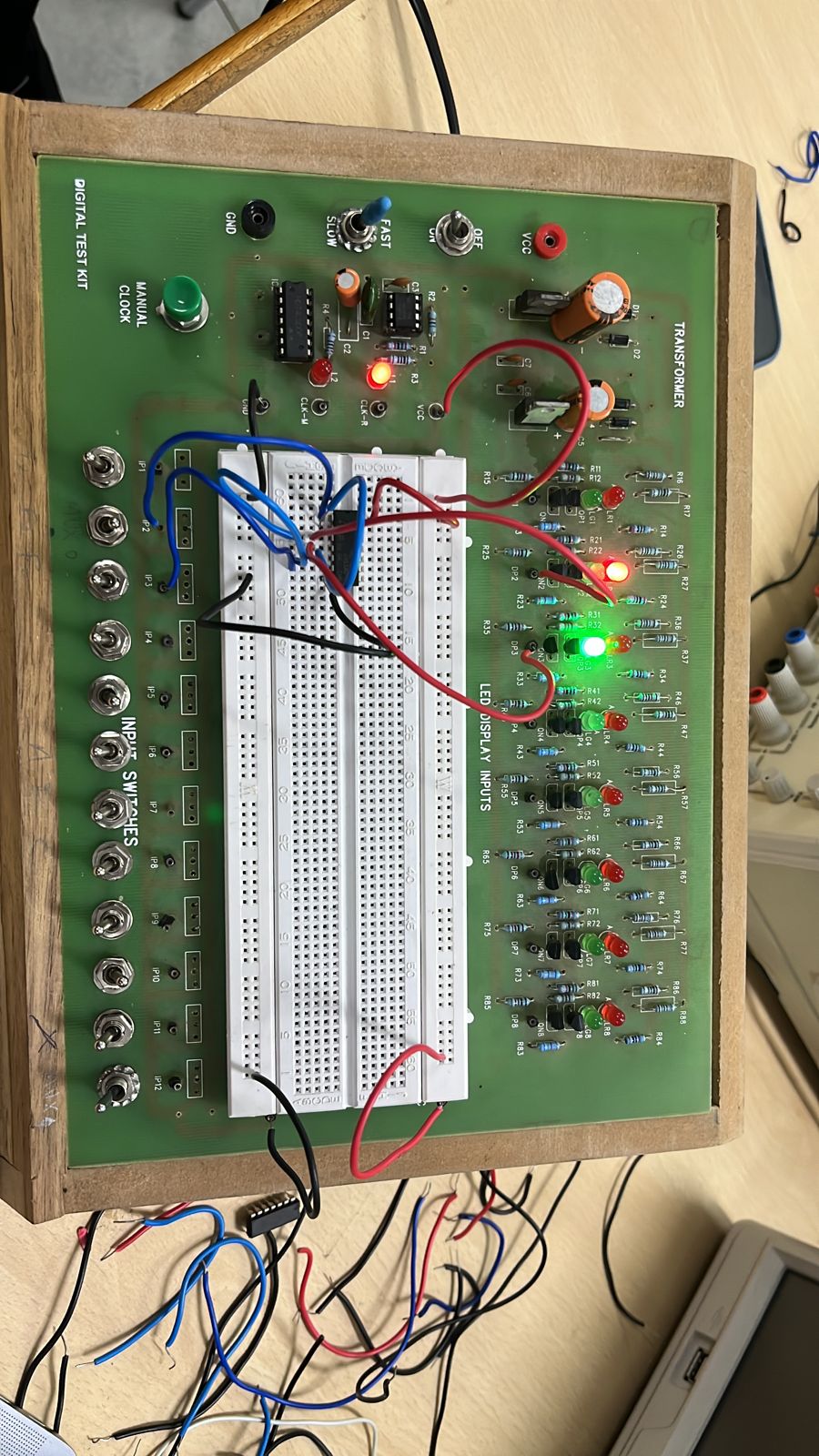
Observation table:-

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | S | R | Q | Q’ |
| 1 | 0 | 1 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 |
| 3 | 1 | 0 | 1 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 1 | 0 | 1 | 0 |
| 7 | 0 | 1 | 0 | 1 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 1 | 0 | 0 |
| 10 | 0 | 0 | 0/1 | 1/0 |
| 11 | 1 | 0 | 1 | 0 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 0 | 0 | 0/1 | 1/0 |
| 14 | 0 | 1 | 0 | 1 |
| 15 | 1 | 1 | 0 | 0 |
| 16 | 0 | 0 | 0/1 | 1/0 |

The possibility of 2 outputs when SR transition from 11 to 00 is because we cannot determine the intermediate state i.e (10 or 01) and changing to 00 from 11 simultaneously is not possible..

SR LATCH output table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | S | R | Q | Q’ |
| 1 | 0 | 0 | Retains the previous output | Retains the previous output |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 1 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0(Forbidden) | 0((Forbidden) |



CONCLUSION:-

Thus in this way we can make SR Latch using NOR gates ..

Experiment 5B:-

To assemble JK Master-Slave Flip flop

Electronic components required:-

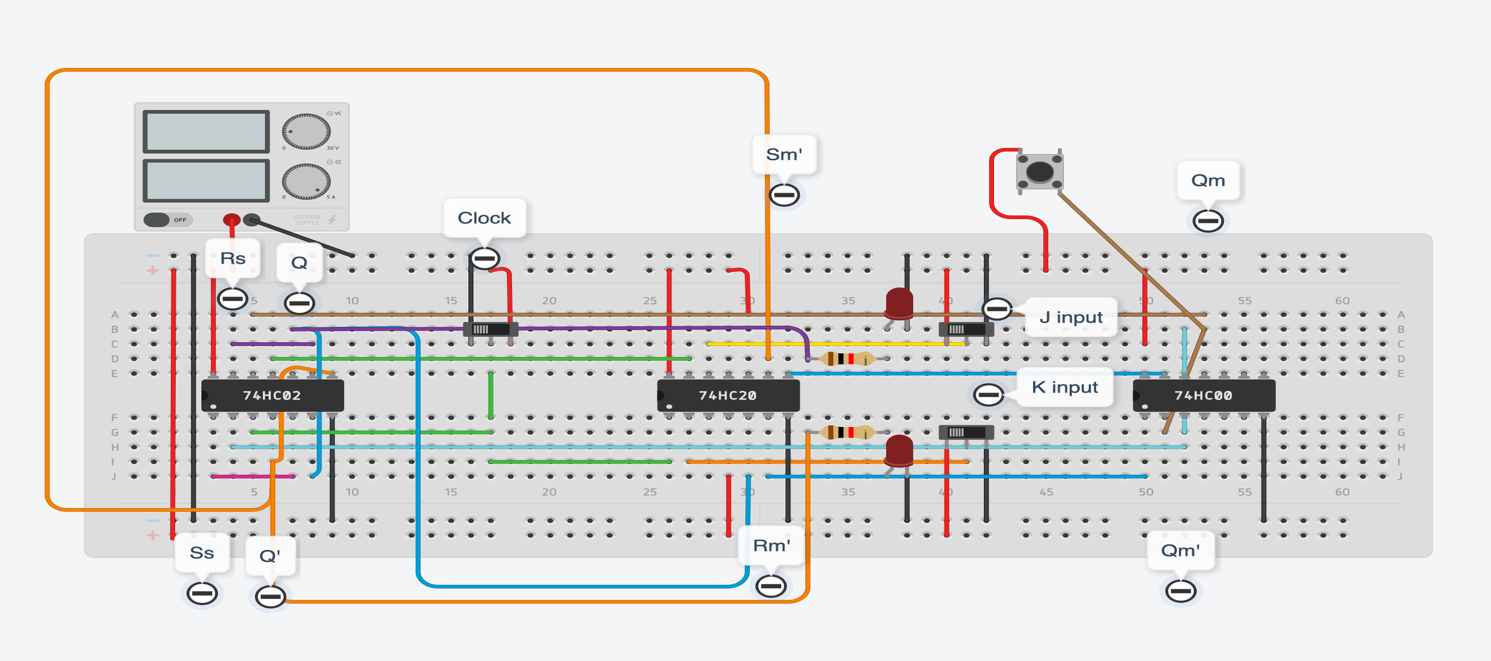
1. Digital test kit
2. Wires
3. NOR gate
4. NAND gate( 2 and 4 input)

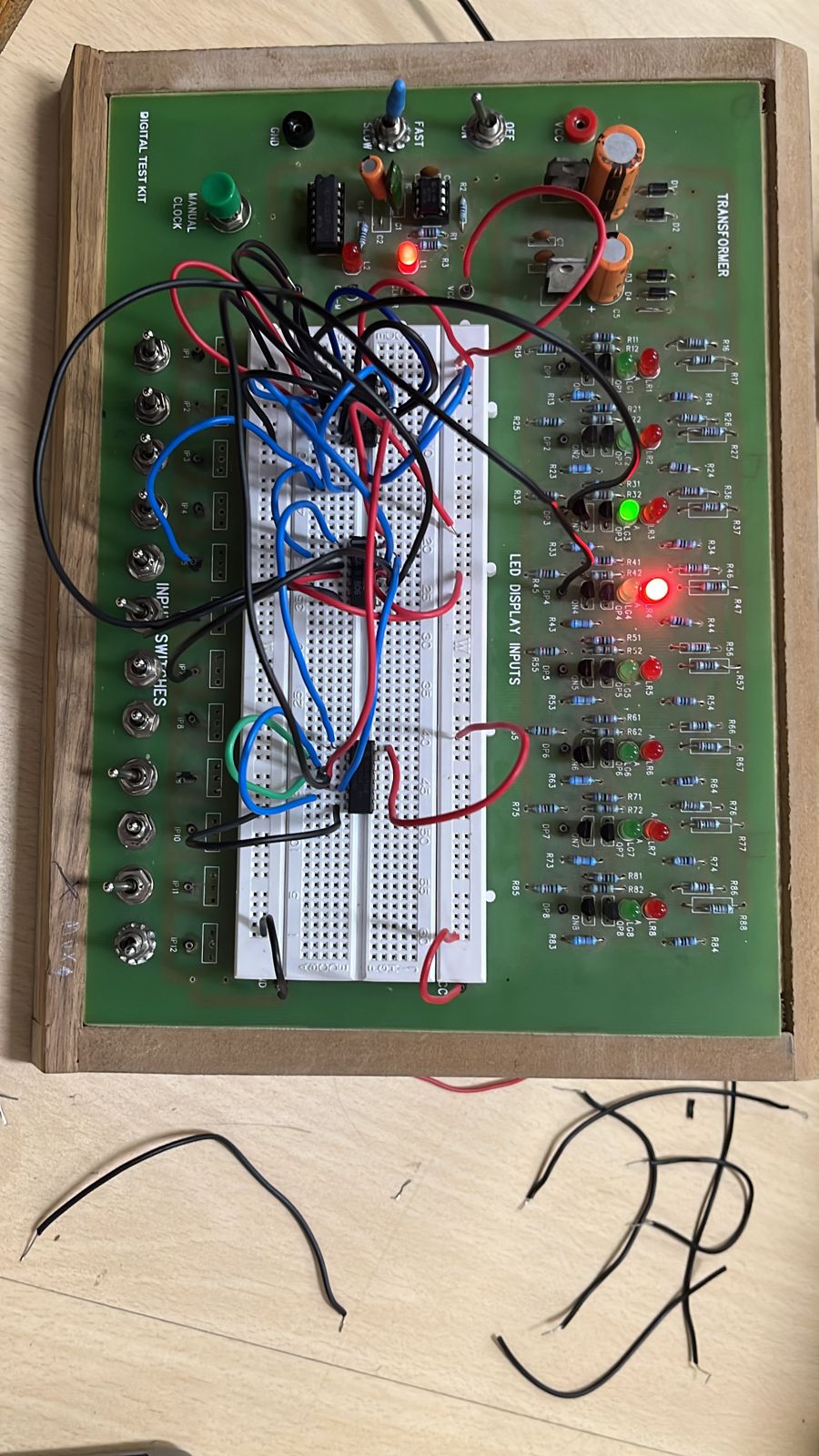
Reference circuit:-

Diagram

Description automatically generated

TinkerCAD screenshot:-





Procedure-

1. Assemble the circuit as shown below. By using two 4-input NAND gates from a CD4012 chip as 3-input gates. Connect the unused inputs of the 4-input NAND gates to the HIGH (VCC) level.
2. Use two input switches to take inputs for R and S latch.
3. Connect the outputs Q and Q’ to two display pins.

Observation table:-

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S.No | J | K | ACTION | Q(t+1) |
| 1 | 0 | 0 | HOLD | Q(t) |
| 2 | 0 | 1 | CLEAR | 0 |
| 3 | 1 | 0 | SET | 1 |
| 4 | 1 | 1 | TOGGLE | Q’(t) |

Conclusion:-

This way we can make a JK flipflop using normal logic gates and feedback mechanism..